REMARKS

The title, specification and drawings have been amended to make editorial changes therein, bearing in mind the criticisms in the Official Action, to place the application in condition for allowance at the time of the next Official Action.

Paragraph 4 of the Official Action states that the steps in the method claims were not considered. This is not understood, in view of the comments about the method claims in subsequent paragraphs. Further, the comment that "power model" equates to "power source" is also not understood. The power model is the model that is described in the specification and is the subject of claim 1; a power source has not been described or claimed.

The specification has been reviewed and amended, taking into consideration the comment regarding §112, first paragraph. It is noted that the claims were not rejected on this basis. The term "power current" is explained without adding new matter. As is known, current (amps) is power (watts) divided by voltage, and thus the presence of a current attributable to the power will be understood by those of skill in the art. Reconsideration and withdrawal of the objection to the specification are respectfully requested.

The claims were rejected under §112, second paragraph, and have been amended as to form, bearing in mind the comments in paragraphs 7-10 of the Official Action. In addition, various other editorial changes have been made to more closely conform to

AMENDMENTS TO THE DRAWINGS:

The replacement drawing sheets in the Appendix include changes to Figures 8-24. These sheets replace the original sheets including Figures 8-24. The spelling of "information," "capacitor," and "capacitors" has been corrected, "average in" has been changed to "average of," and "terminal" has been added after "power."

U.S. practice. Reconsideration and withdrawal of the rejection under §112, second paragraph, are respectfully requested. The term "semiconductor" has been deleted from the claims and the specification. This change is not a narrowing amendment as the meaning of the claims has not changed. As noted in the Official Action, an integrated circuit is defined as a small electronic device made out of a semiconductor material, and thus the use of "semiconductor" is redundant; removal of a redundant term is not a material change to the claims.

Claims 1-116 were rejected as unpatentable over EIAJ ED -5302 of March 31, 1998 (hereinafter "EIAJ") in view of JYU et al. 5,880,967. Reconsideration and withdrawal of the rejection are respectfully requested.

EIAJ discloses a standard interface model for an integrated circuit. In other words, it describes a program. The reference does not describe the hardware on which the program is to be run, and thus does not disclose a logic gate circuit part representing an operating part of the integrated circuit. The Official Action points to the discussion of the MOS transistor on pages 13 and 19, which is a description of the program that models a MOS transistor in the integrated circuit. There is nothing here that describes a piece of hardware, such as a logic gate circuit part, representing an operating part of the integrated circuit. Accordingly, EIAJ does not disclose the claimed logic gate circuit part representing an operating part of the integrated circuit.

The Official Action acknowledges that EIAJ does not disclose the equivalent internal capacitive part representing a non-operating part of the integrated circuit, and relies on JYU et al. for the suggestion to modify the EIAJ model to include this feature, pointing to column 28, lines 10-14 of JYU et al. JYU et al. describes a method for minimizing signal delay and power consumption through transistor sizing. An iterative technique is used to reach an optimum transistor size for acceptable signal delay and power consumption. The cited section of JYU et al. describes a cell selection process in which groups of transistors (a cell) are inserted into the integrated circuit using the delay and power requirements as guides for selecting from among several cells in a cell library. Once a cell has been chosen, it is simply inserted into the integrated circuit (column 27, line 59 through column 28, line 8). In other words, the integrated circuit is designed by selecting and inserting a predefined cell of transistors that provides the required power and delay. A cell is characterized by, among other features, a capacitance. However, JYU et al. does not describe a power model at all and does not describe an equivalent capacitive part representing a non-operating part of the integrated circuit being modeled. The cell does not represent a part of the integrated circuit, it is a part of the integrated circuit and an operating part at that. Accordingly, JYU et al. does not describe the claimed equivalent internal capacitive part and thus does not

motivate one of skill in the art to modify the EIAJ model to include this feature.

Since the two references do not describe the above-noted features of claim 1, this claim and claims 2-20 dependent therefrom avoid the rejection under §103. This traversal also applies to claims 99-116 that include similar limitations.

Claim 21 has been amended to more clearly define the method in which the logic gate circuit part and the equivalent internal capacitive part are prepared taking into account the respective information about operating and non-operating gate circuits. As explained above, the applied references do not disclose the logic gate circuit part and the equivalent internal capacitive part and thus do not describe a method of preparing these parts. Since the references do not describe these features of claim 21, this claim and claims 22-45 dependent therefrom avoid the rejection under §103. This traversal also applies to claims 46-98 that include similar limitations.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any

overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON

Thomas W. Perkins, Reg. No. 33,027
745 South 23rd Street
Arlington, VA 22202
Telephone (703) 521-2297
Telefax (703) 685-0573
(703) 979-4709

TWP/lk

APPENDIX:

The Appendix includes the following items:

- Replacement Sheets for Figures 8-24 of the drawings

- a Substitute Specification and a marked-up copy of the originally-filed specification